Rejections Under 35 U.S.C. §102

Claims 1-3, of which claim 1 is independent, were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,613,162 ("Kabenjian"). The rejection is respectfully traversed.

According to Kabenjian, during initiation, the CPU 100: writes a destination address, size of the transfer and other control data to the DMA controller 202; requests control of the memory bus 110; executes one or more read/write cycles addressed to the IDE device 156; initializes the DMA unit 200; writes to source, destination and count registers A; and writes go and direction data to the command register. See Kabenjian, col. 10, lines 5-61. After setting up the register set A 300 for a first DMA transfer, the CPU 100 either resets the first DMA channel for a second DMA transfer (col. 10, ll. 62-64), or uses a two-deep shadowing technique of "writing appropriate values to register set B of the first register block while the DMA unit is performing the previously initialized DMA transfer" (col. 11, ll. 3-6) or uses multiplexing to quickly switch between register set A or B. (col. 11, ll. 19-21).

In contrast, in claim 1, the DMA controller, not the CPU, *loads the stored parameters* (addressing, counters, pointers to buffer control units, etc.) that enable the data access between the port and the memory. Claim 1 recites (with emphasis added) "wherein the *direct memory access controller stores parameters* defining the direct memory access operations for each port, and wherein after a request is received from a port *the direct memory access controller loads the parameters for a direct memory access operation* responsive to the request from the port to enable the port to access the memory and transfer data between the memory and the buffer associated with the port." In order to emphasize the differences between the claimed invention and Kabenjian's process, claim 1 has been further amended to include the limitation, *and independent of any instruction from a host central processing unit.*

As indicated in the instant Office Action (bottom of page 2), Kabenjian's registers within the DMA unit 200 are set with parameters in response to "a command from the CPU." In contrast, the claims reflect what is described in the application (page 4, ll. 1-21), that "the DMA and BCU controllers impose an autonomous flow control mechanism that ensures that data is

sequenced properly through the processing steps without further attention from the application program."

The Action takes the position that Kabenjian's reference to "selecting" described in and around col. 13, ll. 15-17, is equivalent to the claimed *loading of parameters*. That passage, however, appears to refer to the initial, static loading that is performed by the system BIOS at initialization, taking into account what I/O devices are present in the configuration. In contrast to the presently claimed invention, as described in the instant specification (page 4, ll. 14-21; page 6, ll. 13-15), parameters specific to each channel are stored in DMA controller memory locations (DCBs) that are initially programmed by the application program/CPU, but the claimed *responsive parameter loading* loads parameters for a particular DMA channel dynamically in response to a request from that port.

In response to the further distinguishing amendment made in Applicants' previous response that clarify that the *buffer* in question is *located at and is dedicated to the port*, the Action asserts that this limitation is disclosed in Kabenjian at col. 8, ll. 45-60. The buffers 252-258 are clearly shown in Figs. 1-3 as being incorporated within Kabenjian's DMA unit 200 and described as "preferably" used for transfers with a particular I/O device. In contrast, the recited claims' *buffer located at and is dedicated to the port* is shown as quite distinct from the recited *direct memory access controller* in Applicants' application. For example, Figure 1 and the associated text at page 3, line 6, show the FIFO buffers 112a-112d each located at a separate port and distinct from the DMA controller 116. Similarly, Figure 4 and the text associated therewith at page 4, ll. 25-32, illustrate and describe DMA controller 414 as being distinct from client port FIFO 400. The buffers discussed in the Kabenjian passages, if any similarity exists, may be more like the DMA channels (0-n) and registers 403 that received data from the claimed *port buffers* (client port FIFO buffer 400 in Figure 4.)

Accordingly, in view of the foregoing amendments and remarks, claim 1 is distinguishing from Kabenjian. Dependent claims 2 and 3 are allowable for at least the same reasons

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner

believes, after this reply, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If there is a fee occasioned by this response, including an extension fee, please charge said fee to **Deposit Account No. 50-0876.**

Respectfully submitted,

Avid Technology, Inc.

By_____
John A. Hamilton
Registration No. 48,946
Avid Technology, Inc.
One Park West
Tewksbury, MA 01876
Tel.: (978) 640-6789